CLAIMS

1. A pattern detection apparatus detecting data of a predetermined pattern and saving a position of the detected data among inputted data, comprising:

a plurality of comparison means (122-1 to 122-N) corresponding to the number (N) to be detection targets and pattern detection control means (130), and

detection position registration means (140) having a plurality of holding portions corresponding to the number (M) to be detection targets, wherein

each of a plurality of the comparison means (122-1 to 122-N) has

a detection pattern data holding unit (124) holding data pattern to be a detection target,

a flag holding unit (126) holding a flag signal as information defining a pattern detection window (PDW) corresponding to the data pattern to be a detection target, and

a comparison unit (122) comparing the input data with the data pattern to be a detection target outputted from the detection pattern data holding unit (124) and outputting an agreement signal (HIT) when agreeing,

the flag holding unit (126) outputs a held flag (FLG1) to the pattern detection means (130) when the agreement signal is outputted,

the pattern detection control means (130) generates a pattern detection window signal (PDW) based on a flag signal (FLG) outputted from a comparison unit of each of the comparison means (122-1 to 122-N) and outputs it to the detection position registration means (140) when an agreement signal is outputted from either of a plurality of the comparison means (122-1 to 122-N), and

the detection position registration means (140) holds information showing a position of the inputted data in a plurality of the holding portions sequentially.

2. A pattern detection apparatus as set forth in claim 1, wherein

the pattern detection position control means (130) comprises:

a first logical addition operation circuit (131) operating logical addition of a plurality of agreement signals (first hit signals HIT1) outputted from a plurality of the comparison means (122-1 to 122-N) and outputting a total agreement signal (HIT) in an enable state when either of agreement signal among a plurality

of agreement signals is in an enable state;

a second logical addition operation circuit (132-1) operating logical addition of a plurality of set signals (SET) included in a flag signals (FLG) outputted from a plurality of the comparison means (122-1 to 122-N) and outputting a set signal in an enable state when either of set signal among a plurality of set signals shows an enable state;

a third logical addition operation circuit (132-2) operating logical addition of a plurality of clear signals (CLR) included in a flag signal (FLG) outputted from a plurality of the comparison means (122-1 to 122-N) and outputting a clear signal in an enable state when either of a plurality of clear signals shows an enable state;

pattern detection window signal generation means (133) making the pattern detection window signal (PDW) an active state in response to a set signal in an enable state outputted from the second logical addition operation circuit (132-1) and making the pattern detection window signal (PDW) an inactive state in response to a clear signal in an enable state outputted from the third logical addition operation circuit (132-2), and

a logical addition circuit (134) outputting a

holding enable signal (HEB) when a pattern detection window signal (PDW) outputted from the pattern detection window signal generation means (133) is in an enable state and the total agreement signal (HIT) outputted from the first logical addition operation circuit (131) is in an enable state.

3. A pattern detection apparatus as set forth in claim 1 or 2, wherein

the detection position registration means (140) comprises registers corresponding to the number of patterns of the detection targets.

4. A pattern detection apparatus as set forth in claim 1 or 2, wherein

the detection position registration means (140) is memory means having a capacity corresponding to the number of patterns of the detection targets.

5. A pattern detection apparatus as set forth in either of claims 1 to 4, wherein

the input data is moving image data and audio data compressed and coded in accordance with the MPEG standard.

6. A pattern detection apparatus as set forth in claim 4, wherein

the detection target pattern is set in response to identification data showing a head of a

packets included in data compressed and coded in accordance with the MPEG standard.

7. A pattern detection circuit comprising:

detection pattern storage means holding an entry pattern to be a detection target;

flag storage means storing a flag signal corresponding to each of the entry pattern;

comparison means comparing inputted data with an entry pattern stored in the detection pattern storage means, and

detection position storage means storing the detection position in response to a flag signal corresponding to the entry pattern stored in the flag storage means when the input data and the entry pattern agree as a result of a comparison of the comparison means.

8. A pattern detection circuit as set forth in claim 1, further comprising:

detection position storage control means setting a pattern detection window signal in an active state when the flag signal corresponding to the entry pattern shows to store a detection position, and setting the pattern detection window signal in an inactive state when the flag signal corresponding to the entry pattern shows not to store a detection position in the case of judged that the input data and the entry pattern agree by

the comparison means.

9. A pattern detection circuit as set forth in claim 2, wherein

the detection position storage means stores a detection position of the entry pattern when the pattern detection window signal is in an active state, and does not store a detection position of the entry pattern when the pattern detection window signal is in an inactive state.

10. A pattern detection circuit as set forth in claim 1, wherein

the input data is moving image data and audio data compressed and coded in accordance with the MPEG standard.

11. A pattern detection apparatus as set forth in claim2, wherein the entry pattern is set in response to identification data showing a head of packets included in the compressed and coded data.